WHAT IS CLAIMED IS:

1. A method of compacting a circuit layout comprising:

determining a critical path of a circuit layout;

performing an automated nonobject-increasing operation with respect to an object in the critical path for decreasing a size of the object in a direction of the critical path.

2. The method of claim 1 wherein the automated nonobject-increasing operation decreases the size of the object in the critical path by rotating the object.

3. The method of claim 1 wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by reshaping the object.

4. The method of claim 1 wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by redistributing at least a portion of the object.

5. The method of claim 1 wherein the performing the automated nonobject-increasing operation includes performing an object rotation operation on an object in the critical path.

6. The method of claim 5 wherein the object includes an interconnect pad.

7. The method of claim 5 wherein the object rotation operation includes:

rotating the object in the circuit layout.

8. The method of claim 7 wherein the object rotation operation further comprises:

determining whether the rotation of the object reduces the critical path.

9. The method of claim 7 wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is parallel with a compaction direction of the automated nonobject-increasing operation.

10. The method of claim 1 wherein the performing the automated nonobject-increasing operation includes performing an object redistribution operation on an object in the critical path.

11. The method of claim 10 wherein the performing the object redistribution operation includes performing a transistor width portion redistribution operation on a transistor width portion in the critical path.

12. The method of claim 11 wherein the performing the transistor width redistribution portion operation includes performing a transistor finger removing operation on a transistor finger in the critical path.

13. The method of claim 12 wherein the transistor finger is part of a logical transistor of the circuit layout, wherein the transistor finger removing operation includes redistributing the transistor finger to at least one other transistor finger of the logical transistor.

14. The method of claim 13 wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger removing operation further comprises:

leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed.

15. The method of claim 11 wherein the transistor width portion is part of a logical transistor of the circuit layout, the transistor width portion redistribution operation further comprises redistributing at least a portion of the transistor width portion to another transistor finger of the logical transistor.

16. The method of claim 15 wherein the transistor width portion redistribution operation further comprises:

determining whether the redistribution of the at least a portion of the transistor width portion reduces the critical path.

17. The method of claim 16 wherein the transistor width portion redistribution operation further includes restoring the at least a portion of the transistor width portion in the circuit layout if the redistribution is determined not to reduce the critical path in the determining.

18. A method of compacting a circuit layout comprising:

determining a critical path of a circuit layout;

performing an automated transistor width portion redistribution operation on a transistor width portion in the critical path for reducing the critical path.

19. The method of claim 18 wherein the transistor width portion is a transistor finger of a logical transistor of the circuit layout, the automated transistor redistribution operation further includes:

redistributing at least a portion of the transistor finger to at least one other transistor finger of the logical transistor.

20. The method of claim 19 wherein the redistributing further includes:

redistributing the transistor finger to at least one other transistor finger of the logical transistor.

21. The method of claim 20 wherein the transistor finger is located on the end of a transistor chain of the circuit layout.

22. The method of claim 20 wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger redistribution operation further comprises:

leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed.

23. The method of claim 20 wherein the transistor finger redistribution operation further

includes redistributing a second transistor finger.

24. The method of claim 23 wherein the transistor finger and the second transistor finger are part of the same logical transistor of the circuit layout.

25. The method of claim 23 wherein the transistor finger is part of a first logical transistor and the second transistor finger is part of a second logical transistor.

26. The method of claim 19 wherein the redistributing at least a portion of the transistor finger to at least one other transistor finger further includes adding at least a portion of the at least a portion of the transistor finger to a transistor finger of the at least one transistor finger thereby increasing a width of the transistor finger of the at least one transistor finger, wherein the width of the transistor finger of the at least one transistor finger is in a direction generally parallel to a compaction direction of the automated transistor redistribution operation.

27. The method of claim 18 wherein the transistor width portion is part of a logical transistor, wherein the automated transistor redistribution operation further includes:

creating a new transistor finger;

moving at least a portion of the transistor width portion to the new transistor finger.

28. A method of compacting a circuit layout comprising:

determining a critical path of a circuit layout;

performing at least one of an object redistribution operation on an object in the critical path and an automated object rotation operation on an object in the critical path for compacting the circuit layout.

29. The method of claim 28 wherein the performing further includes performing an object rotation operation on an object in the critical path.

30. The method of claim 29 wherein the automated object rotation operation includes:

rotating the object in the circuit layout.

31. The method of claim 30 wherein the automated object rotation operation further comprises:

determining whether the rotation of the object reduces the critical path.

32. The method of claim 30 wherein the object includes an interconnect pad.

33. The method of claim 30 wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is parallel with a compaction direction of the automated nonobject-increasing operation.

34. The method of claim 28 wherein the operation is a nonobject increasing operation.

35. The method of claim 28 wherein:

the performing further includes performing an object redistribution operation on an

object in the critical path;

the performing the object redistribution operation further includes performing a transistor width portion redistribution operation on a transistor width portion in the critical path.